REMARKS

In the Office Action, the Examiner noted that claims 1-15 are pending in the application and that claims 1-15 are rejected. By this response, claims 1-15 continue without amendment. In view of the following discussion, Applicants submit that none of the claims now pending in the application are anticipated under the provisions of 35 U.S.C. §102. Thus, Applicants believe that all of these claims are now in condition for allowance.

Rejection of Claims Under 35 U.S.C. §102

The Examiner rejected claims 1-15 as being anticipated by Anderson (United States patent 6,871,336, issued March 22, 2005). In particular, the Examiner stated that Anderson discloses generating a new routed design using incremental routing based on results of an incremental placement. (Office Action, p. 2). The rejection is respectfully traversed.

Anderson generally teaches a CAD process for designing an integrated circuit that includes incremental placement. In particular, a design is placed and routed using conventional methods. The design is processed using conventional timing analysis to determine if incremental placement is need. If so, incremental placement is performed resulting in physical placement of design objects on physical positions of the integrated circuit. (Anderson, col. 4, lines 17-39). Routing is then performed to complete the design using any known method of routing. (Anderson, col. 4, lines 40-43).

Anderson, however, does not teach each and every element of Applicants' invention recited in claim 1. Namely, Anderson does not teach or suggest generating a new routed design using incremental routing based on results of incremental placement. Rather, Anderson discloses conventional routing of an incrementally placed design. Conventional routing, as taught by Anderson, is not equivalent to incremental routing, as recited in Applicants' claim 1. In the conventional routing process, the pins in each net of a logic design are connected (i.e., all of the nets in the logic design are processed). (See, Anderson, col. 1, lines 60-61). In an incremental routing process, only a subset of the nets in a logic design is processed, rather than all

of the nets. Some nets associated with portions of the design that were not affected by the incremental placement process are not processed during the incremental routing process. (See Applicants' specification, p. 16, ¶0044). In Anderson, the incrementally placed design is completely routed each time using a conventional routing process. There is no teaching or suggestion in Anderson of only routing connections for a subset of the nets in the design after the incremental placement process.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir. 1984). Since Anderson does not teach or suggest generating a new routed design using incremental routing based on results of incremental placement, Anderson does not teach each and every element of Applicants' claim 1. Claims 2-15 depend, either directly or indirectly, from claim 1 and recite additional features therefor. Since Anderson does not anticipate Applicants' invention as recited in claim 1, dependent claims 2-15 are also not anticipated and are allowable. Therefore, Applicants contend that claims 1-15 are not anticipated by Anderson and, as such, fully satisfy the requirements of 35 U.S.C. §102. Accordingly, Applicants respectfully request that the rejection of claims 1-15 be withdrawn.

CONCLUSION

Thus, Applicants submit that none of the claims presently in the application are anticipated under the provisions of 35 U.S.C. §102. Consequently, Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring any adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Kim Kanzaki at (408) 879-6149 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

Respectfully submitted,

Kim Kanzaki, Ph.D.
Attorney for Applicants
Reg. No. 37,652

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on December 19, 2005 .

Pat Tompkins
Name

Signature